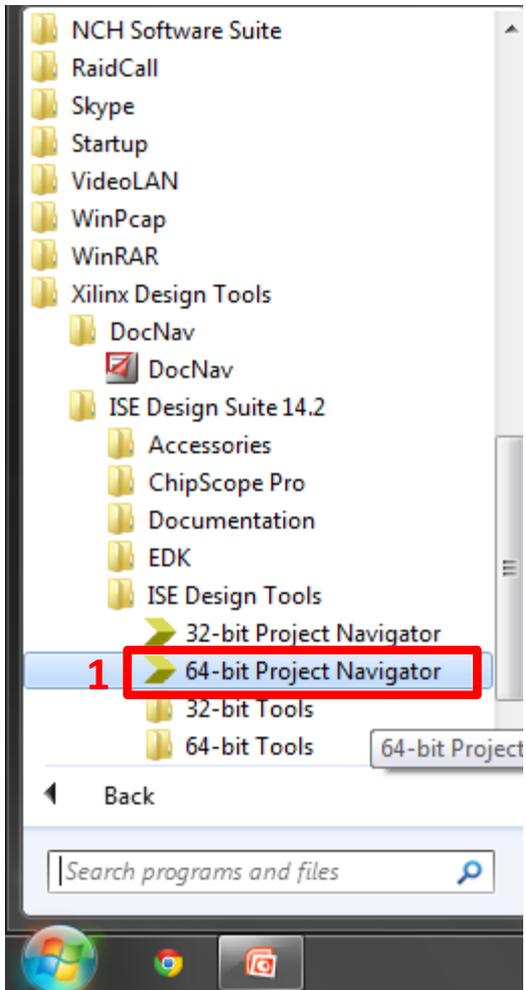
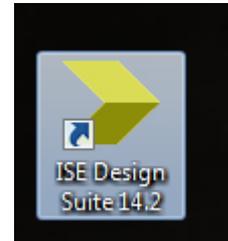


Fazer um Projecto no XILINX

1- Abrir o ISE Design Suite 14.2, através do icon no Desktop ou através da barra de programas.



1



2- Criar um novo projecto

The screenshot shows the Xilinx ISE Project Navigator interface. The 'File' menu is open, and the 'New Project...' option is highlighted with a red box. The main window displays the Design Summary for a project named 'teste1'.

teste1 Project Status

Project File:	Teste.xise	Parser Errors:	No Errors
Module Name:	teste1	Implementation State:	New
Target Device:	xc7a100t-3csg324	Errors:	
Product Version:	ISE 14.2	Warnings:	
Design Goal:	Balanced	Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	
Environment:		Final Timing Score:	

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report					
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports

Report Name	Status	Generated
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Date Generated: 10/20/2012 - 16:19:34

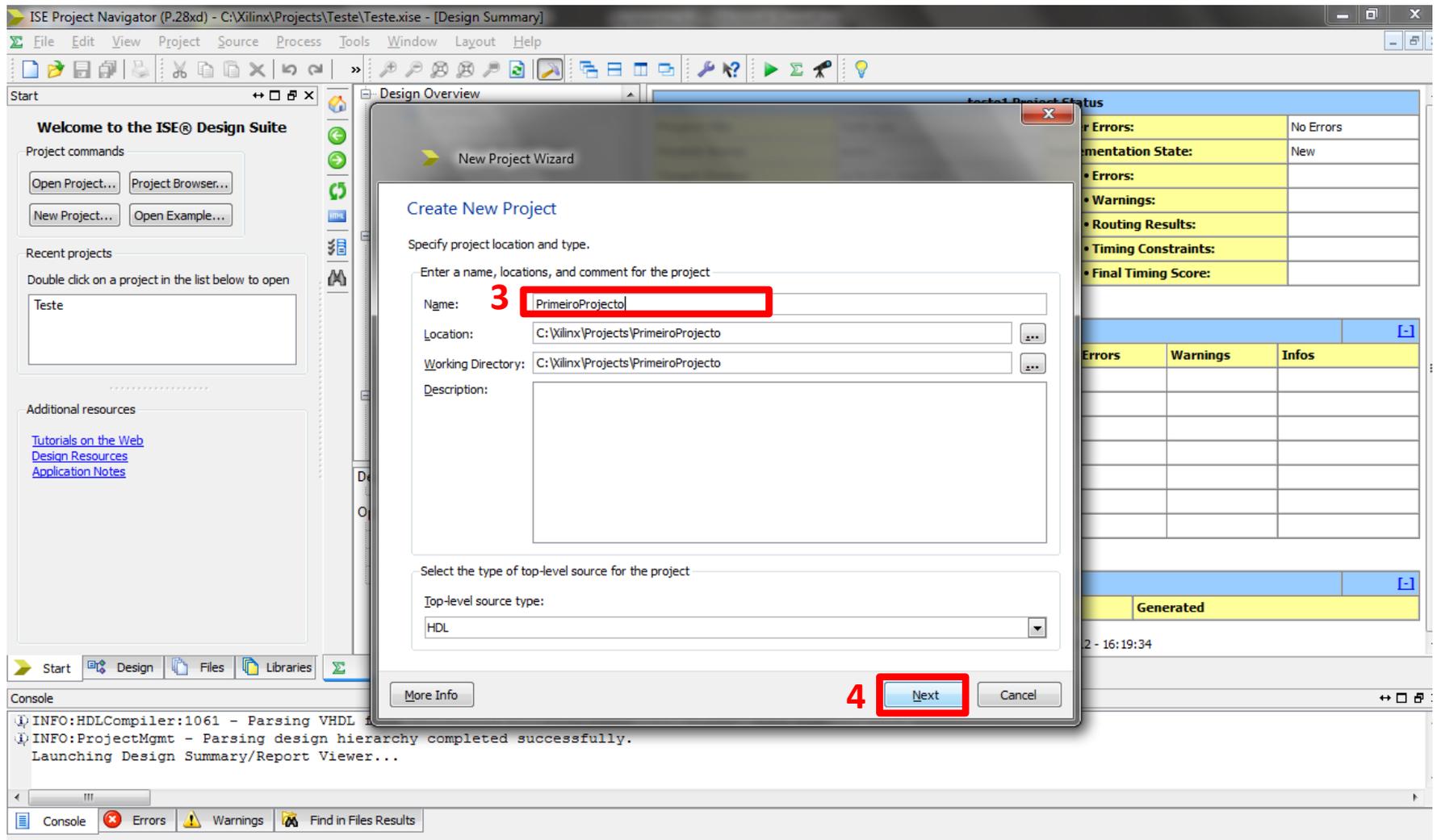
Console

```
INFO:HDLCompiler:1061 - Parsing VHDL file "C:/Xilinx/Projects/Teste/teste1.vhd" into library work
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Launching Design Summary/Report Viewer...
```

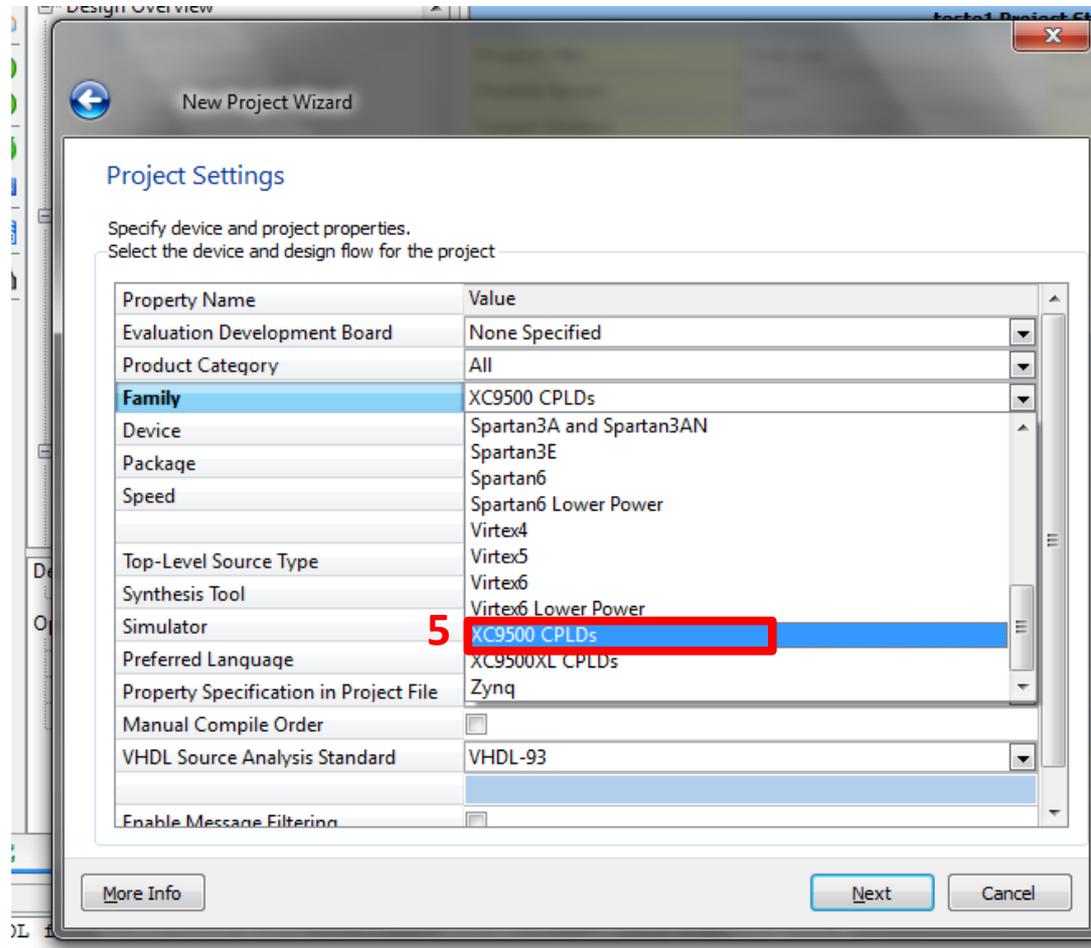
Create a new project

3-Dar o nome ao projecto

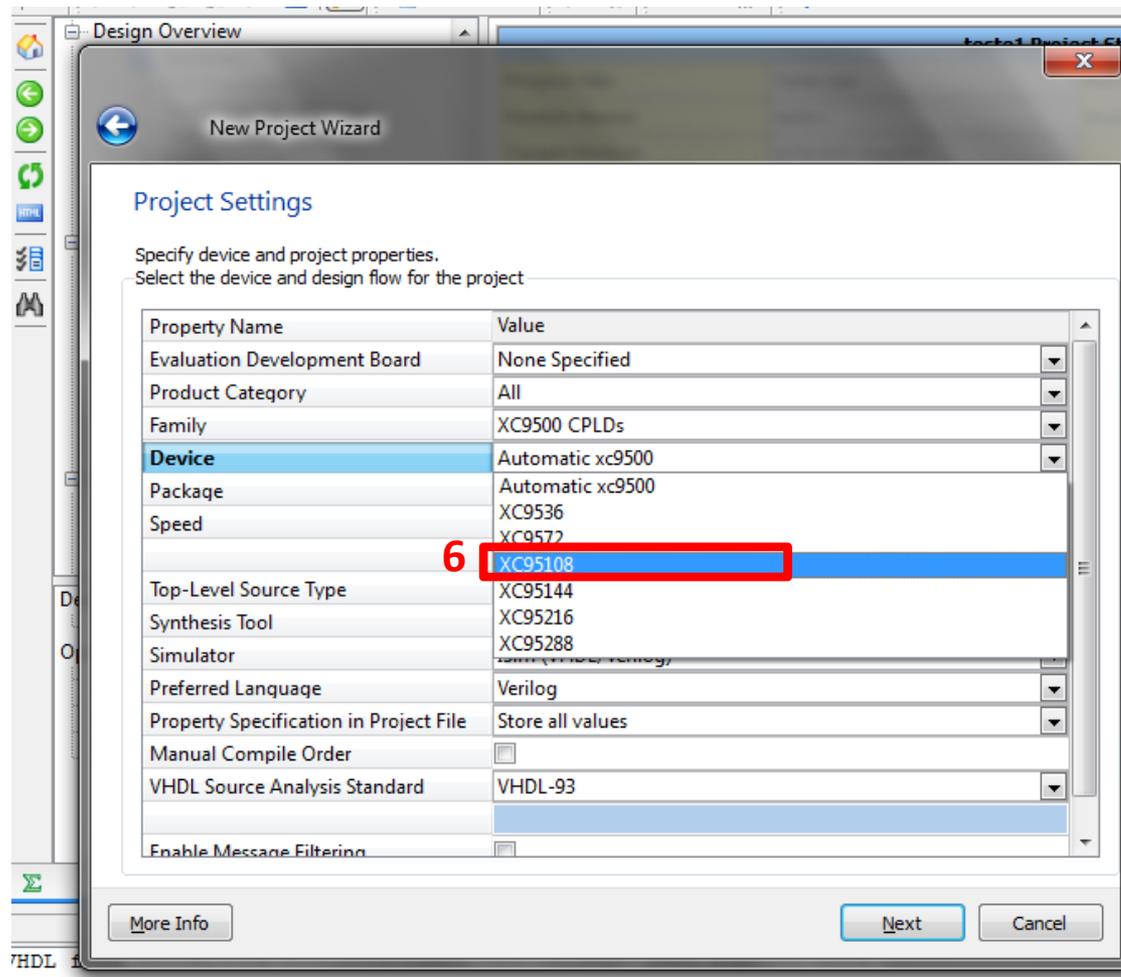
4- Next



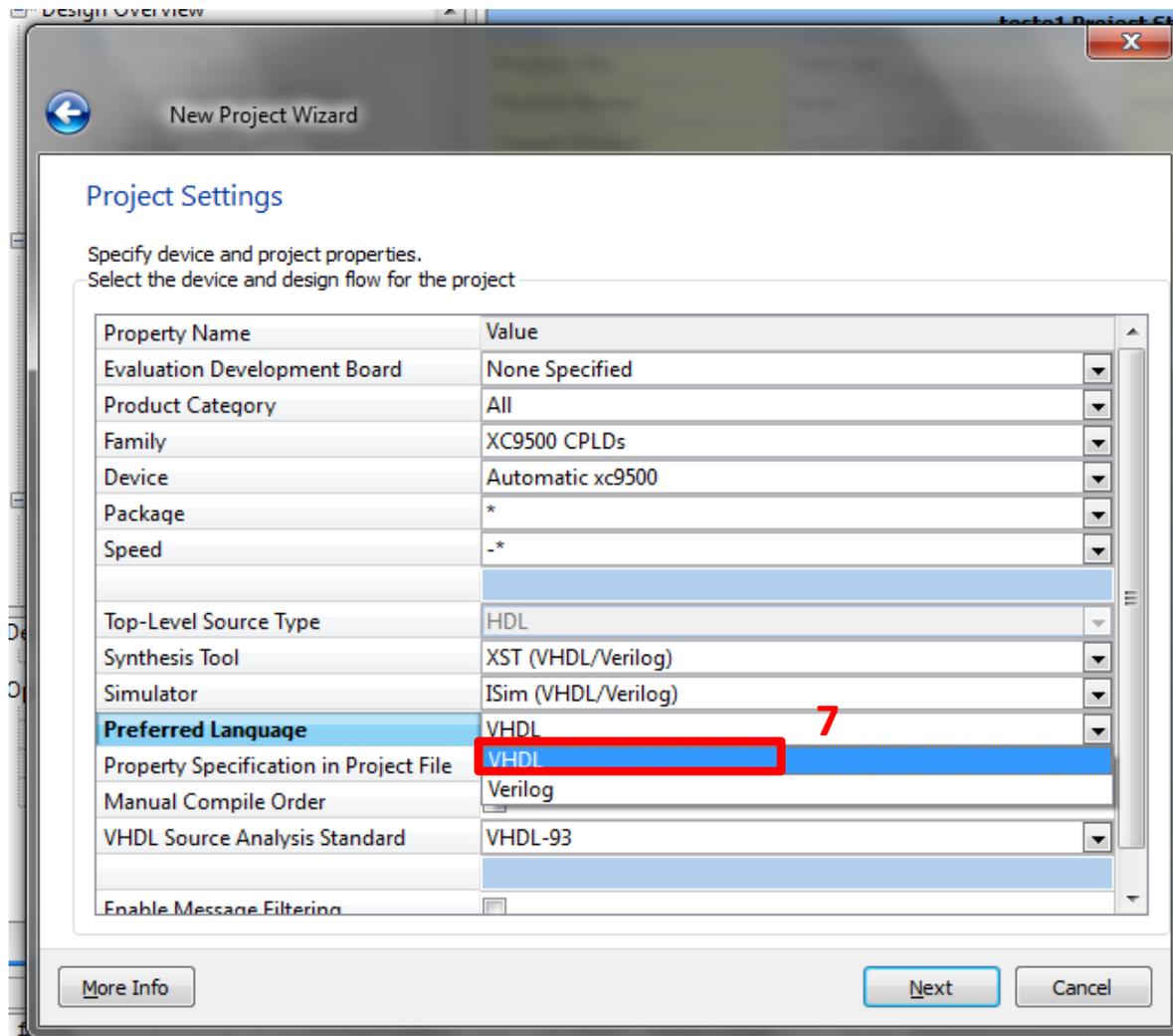
5- No campo Family escolher XC9500 CPLDs



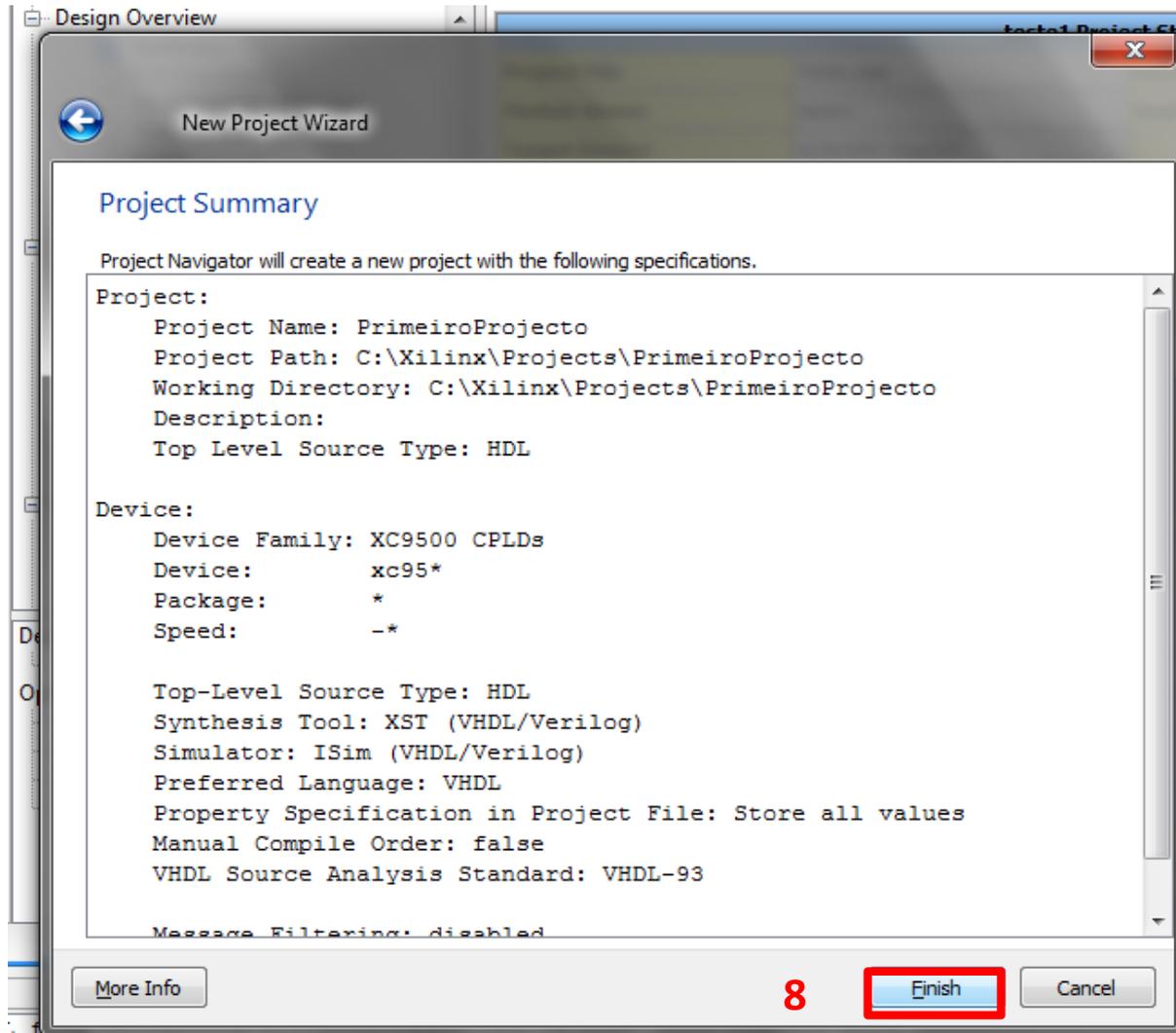
6- No campo Device escolher o XC95108



7- No campo Preferred Language escolher VHDL



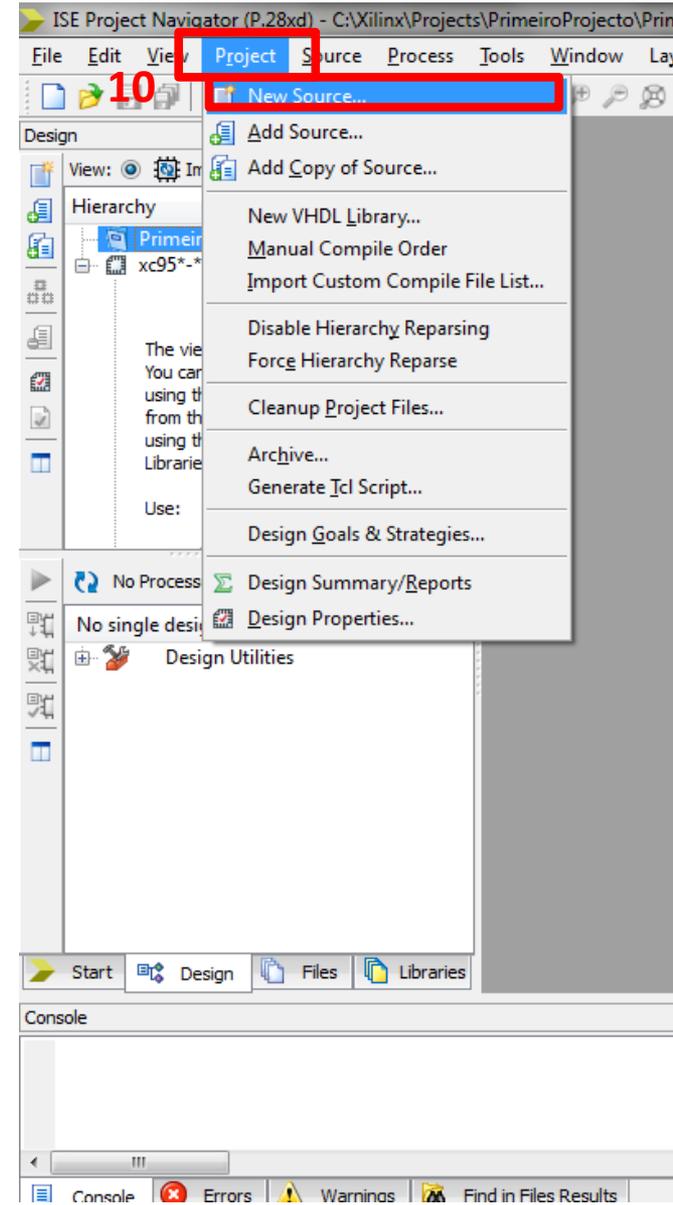
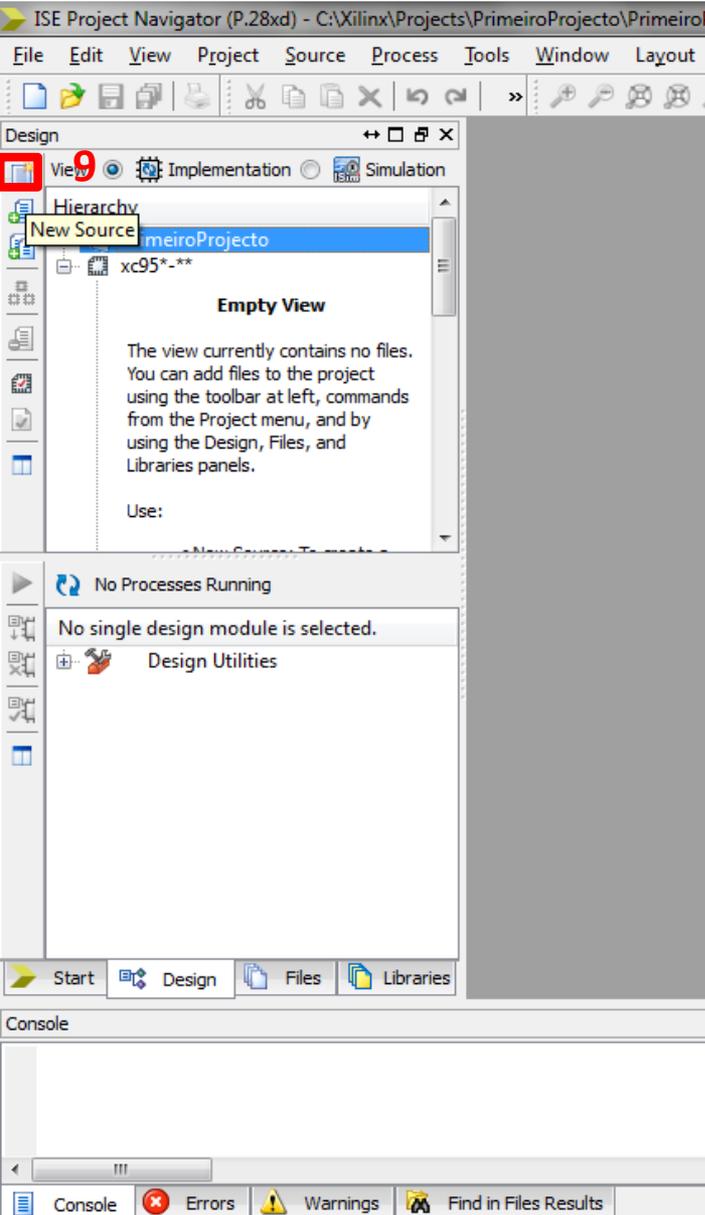
8- Finish



9- Clicar no botao New Source

OU

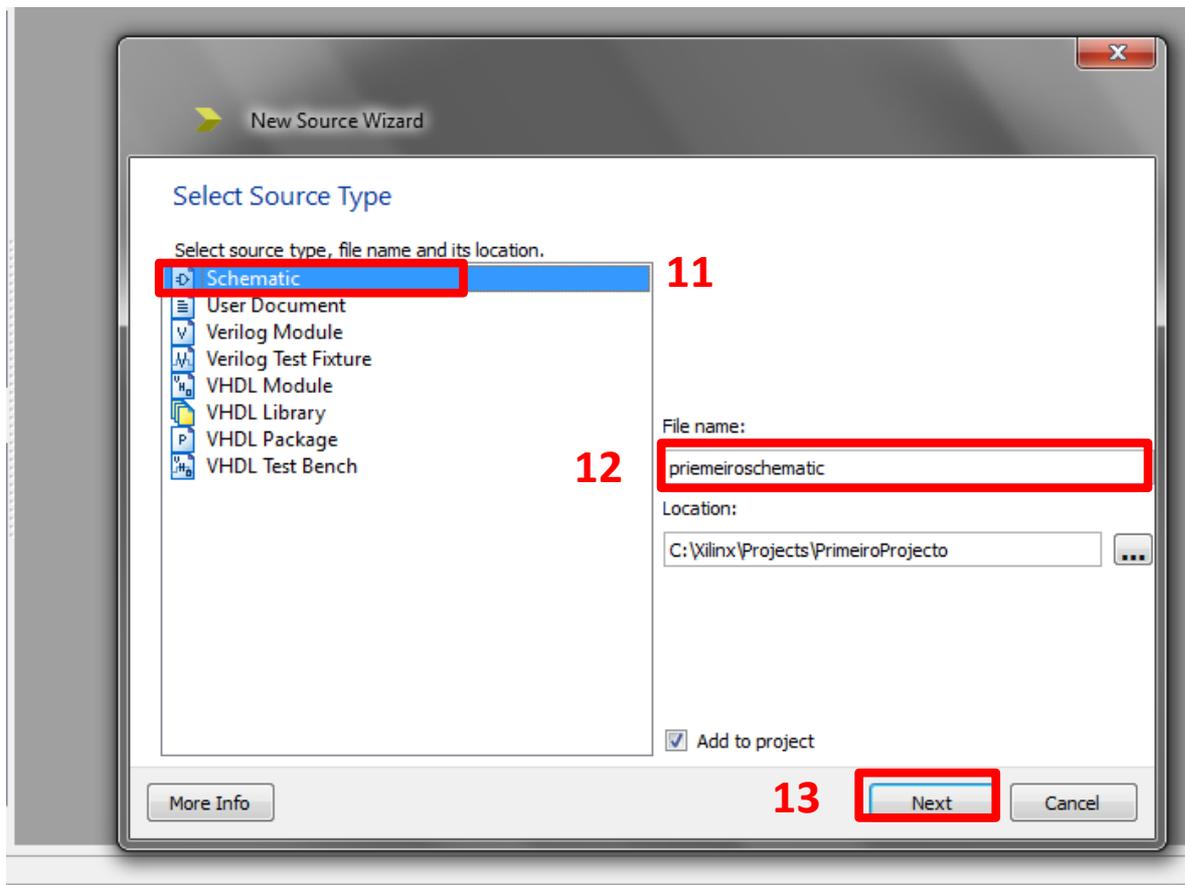
10- Em Project, clicar em New Source



11- Escolher Schematic para criar um esquemático

12- Dar um nome ao ficheiro

13- Next



14- Clicar na tab de Symbols, e escolher que simbolos colocar.

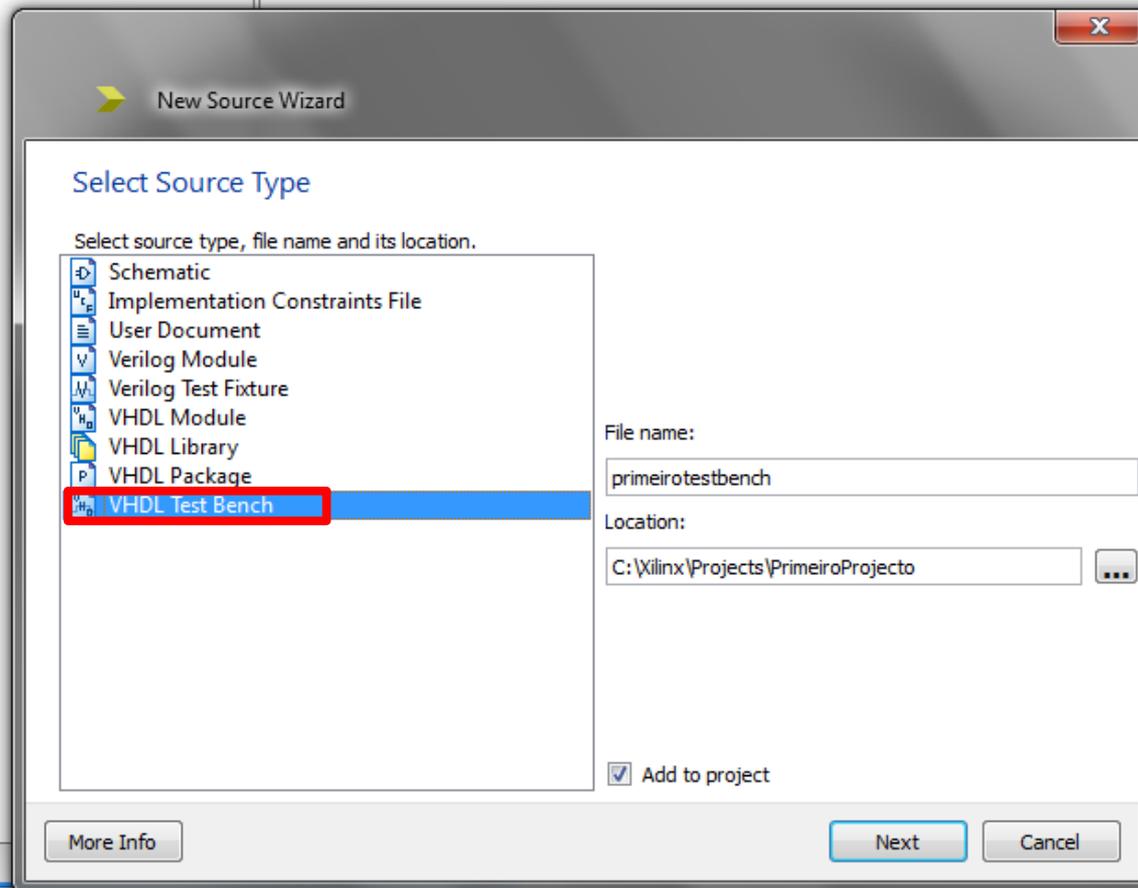
15- Exemplo: escolher Logic e depois uma and2 (And 2 entradas)

The screenshot displays the Xilinx ISE Project Navigator interface. The main window is the Schematic Editor, showing a logic circuit on a grid. The circuit consists of three inputs: A, B, and C. Input A and B are connected to an AND2 gate. Input C is connected to an INV (inverter) gate. The output of the AND2 gate and the output of the INV gate are connected to an OR2 gate, which produces the final output F. The Symbols library is open on the left, showing the 'Logic' category selected (highlighted with a red box and labeled '15'). Within the 'Logic' category, the 'and2' symbol is selected (also highlighted with a red box and labeled '15'). At the bottom of the interface, the 'Symbols' tab is selected (highlighted with a red box and labeled '14'). The Console window at the bottom shows the following text: "Started : \"Launching Schematic Editor to edit priemeiroschematic.sch\". Launching Design Summary/Report Viewer...".

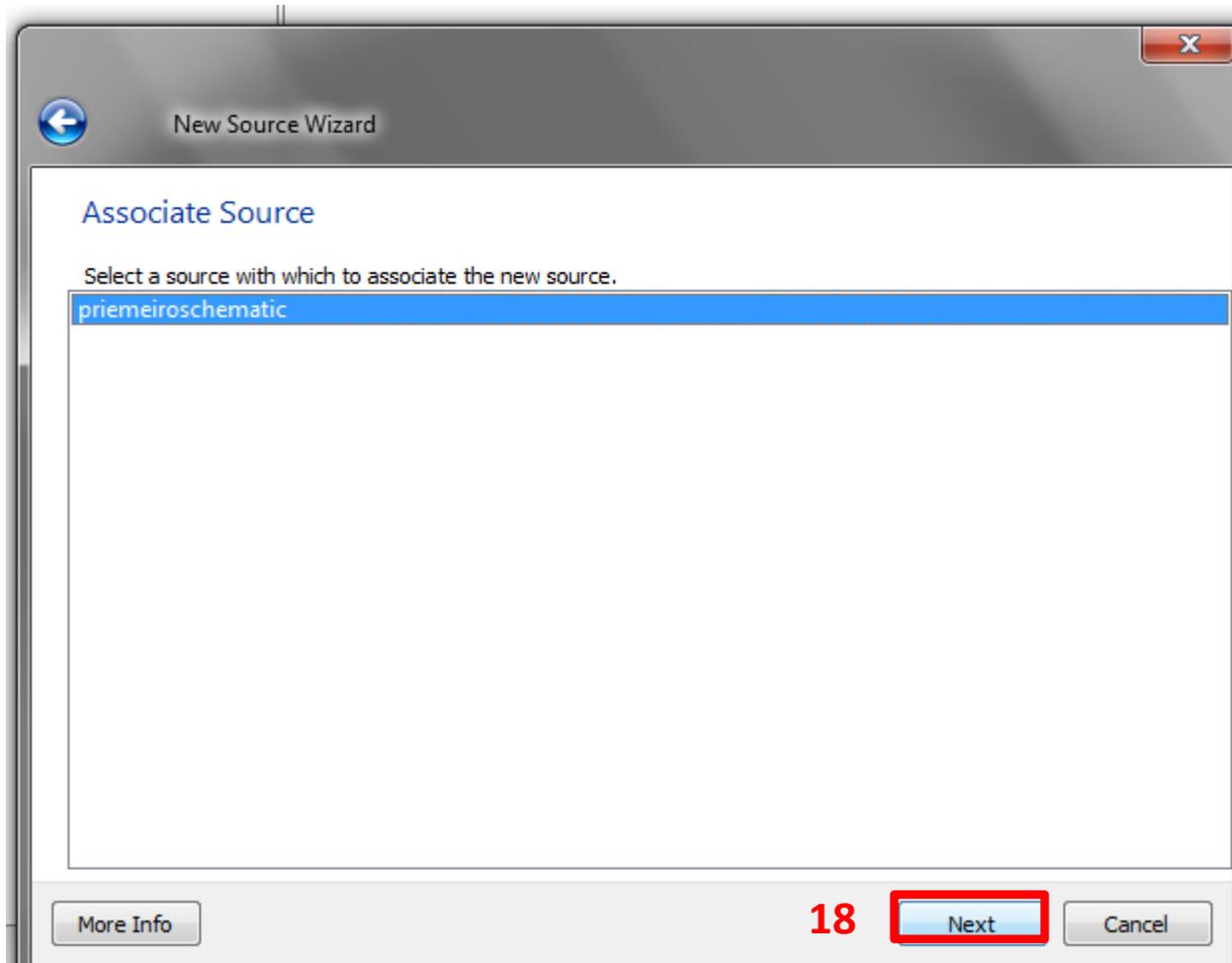
Como criar um ficheiro de simulação

17- Clicar em New Source como feito no passo 9 ou 10, e escolher VHDL Test Bench

17



18- Escolher da lista de esquemáticos o esquemático que queremos simular. (um projecto pode conter vários esquemáticos) e clicar em next. Isso vai criar um ficheiro de simulação em VHDL que vamos ter de modificar.



19- No ficheiro criado é necessário introduzir a evolução das entradas. Um exemplo para 3 bit está apresentado no quadro 19.

The screenshot displays the Xilinx ISE Project Navigator interface. The main window shows the VHDL code for a test bench. A red box highlights the test bench process code, and the number 19 is written next to it. The console shows the simulation results.

```
33     SIGNAL C : STD_LOGIC;  
34     SIGNAL F : STD_LOGIC;  
35  
36     BEGIN  
37  
38     UUT: priemeiroschematic PORT MAP(  
39         A => A,  
40         B => B,  
41         C => C,  
42         F => F  
43     );  
44  
45  
46     -- *** Test Bench - User Defined Section ***  
47     tb : PROCESS  
48     BEGIN  
49         A <= '0'; B <= '0'; C <= '0';  
50         wait for 100 ns;  
51         A <= '0'; B <= '0'; C <= '1';  
52         wait for 100 ns;  
53         A <= '0'; B <= '1'; C <= '0';  
54         wait for 100 ns;  
55         A <= '0'; B <= '1'; C <= '1';  
56         wait for 100 ns;  
57         A <= '1'; B <= '0'; C <= '0';  
58         wait for 100 ns;  
59         A <= '1'; B <= '0'; C <= '1';  
60         wait for 100 ns;  
61         A <= '1'; B <= '1'; C <= '0';  
62         wait for 100 ns;  
63         A <= '1'; B <= '1'; C <= '1';  
64         WAIT; -- will wait forever  
65     END PROCESS;  
66     -- End Test Bench - User Defined Section ***  
67
```

19

ISim simulation engine GUI launched successfully
Process "Simulate Behavioral Model" completed successfully

20- Para obter o gráfico, em Simulation, clicar em Behavioral Check Syntax e depois em Simulate Behavioral Model e uma nova janela aparecerá com o gráfico temporal.

The screenshot displays the Xilinx ISE Project Navigator interface. The main window shows the project hierarchy on the left, the source code in the center, and the simulation process on the right. The source code is as follows:

```
33 SIGNAL C : STD_LOGIC;  
34 SIGNAL F : STD_LOGIC;  
35  
36 BEGIN  
37  
38 UUT: priemeiroschematic PORT MAP(  
39     A => A,
```

The simulation process is shown in the bottom right corner, with the following steps:

- Behavioral Check Syntax
- Simulate Behavioral Model

The timing diagram shows the signals a, b, c, and f over time. The signals are shown as green traces on a black background. The time axis ranges from 0 ns to 1,000,000 ns. The signals a, b, and c are high (1) and signal f is low (0) for most of the duration, with some transitions.

The console output shows the following messages:

```
ISim simulation engine GUI launched  
Process "Simulate Behavioral Model" started  
WARNING: A WEBPACK license was found.  
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.  
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.  
This is a Lite version of ISim.  
Time resolution is 1 ps  
Simulator is doing circuit initialization process.  
Finished circuit initialization process.  
ISim>
```