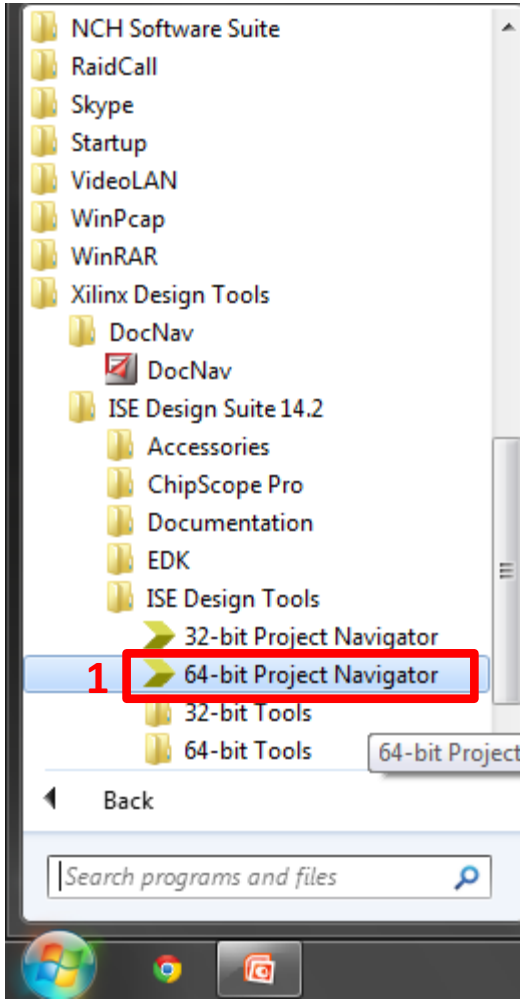
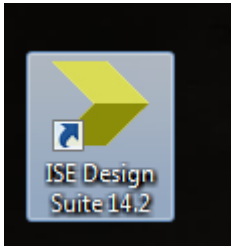
Fazer um Projecto no XILINX

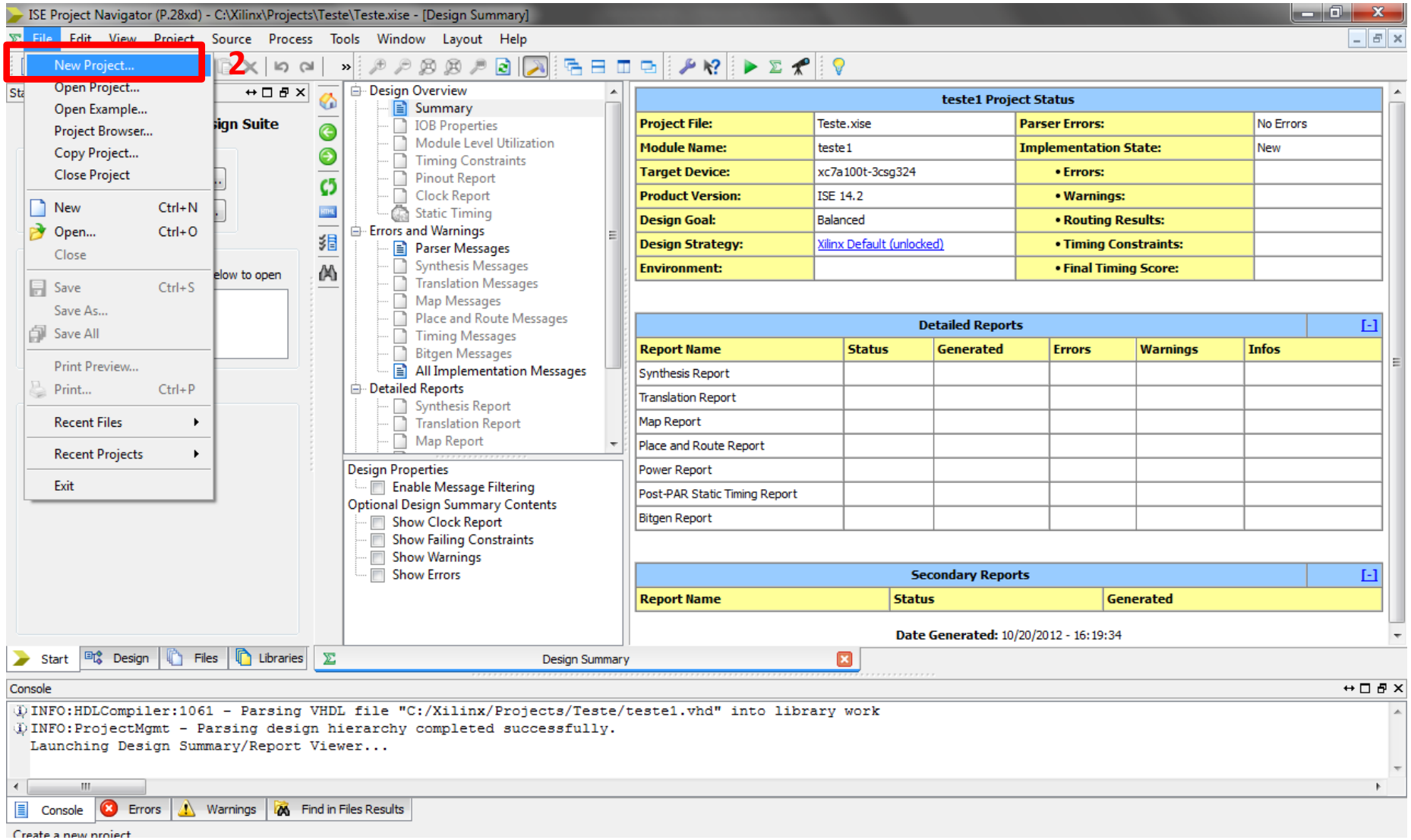


1- Abrir o ISE Design Suite 14.2, através do icon no Desktop ou através da barra de programas.

1

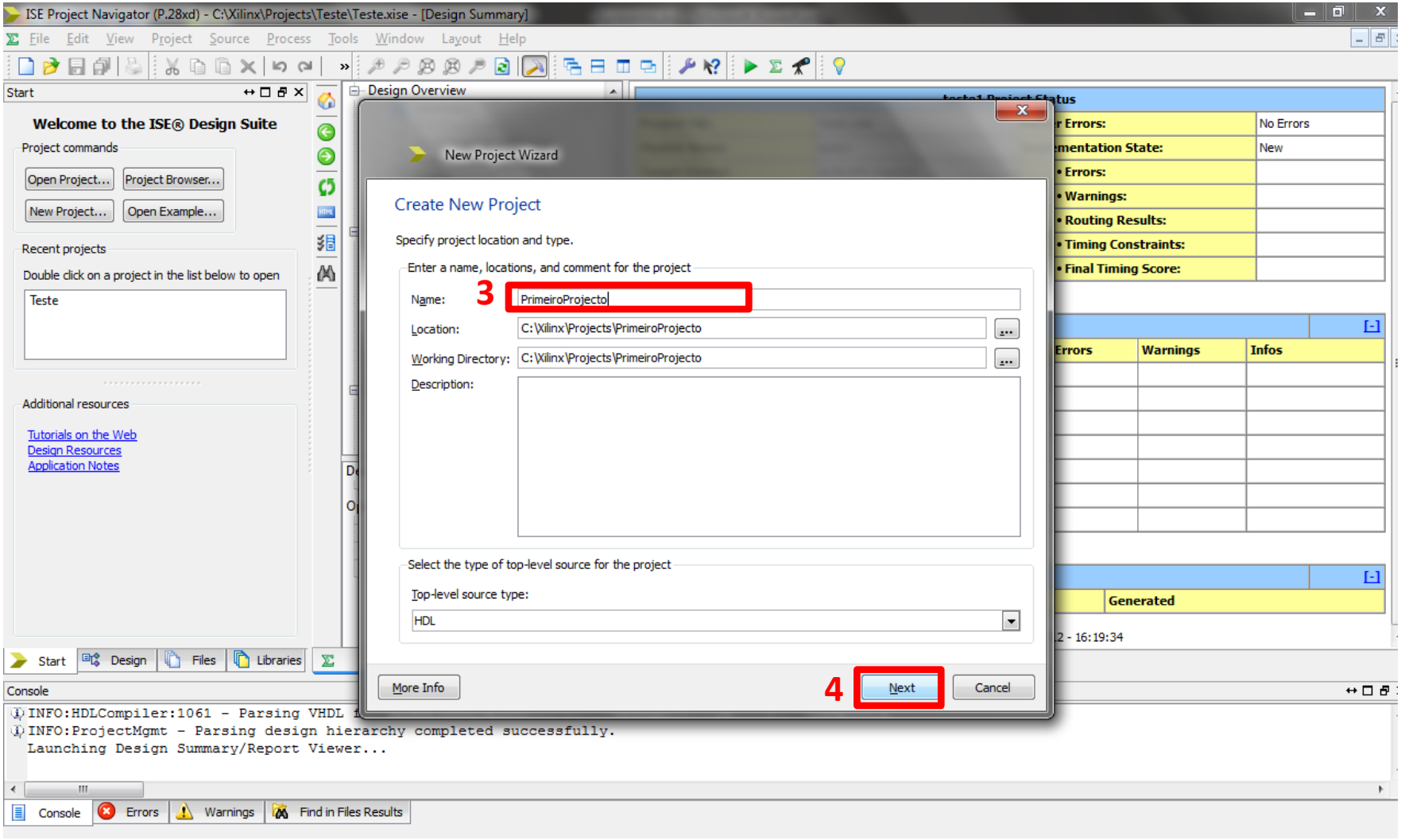


2- Criar um novo projecto

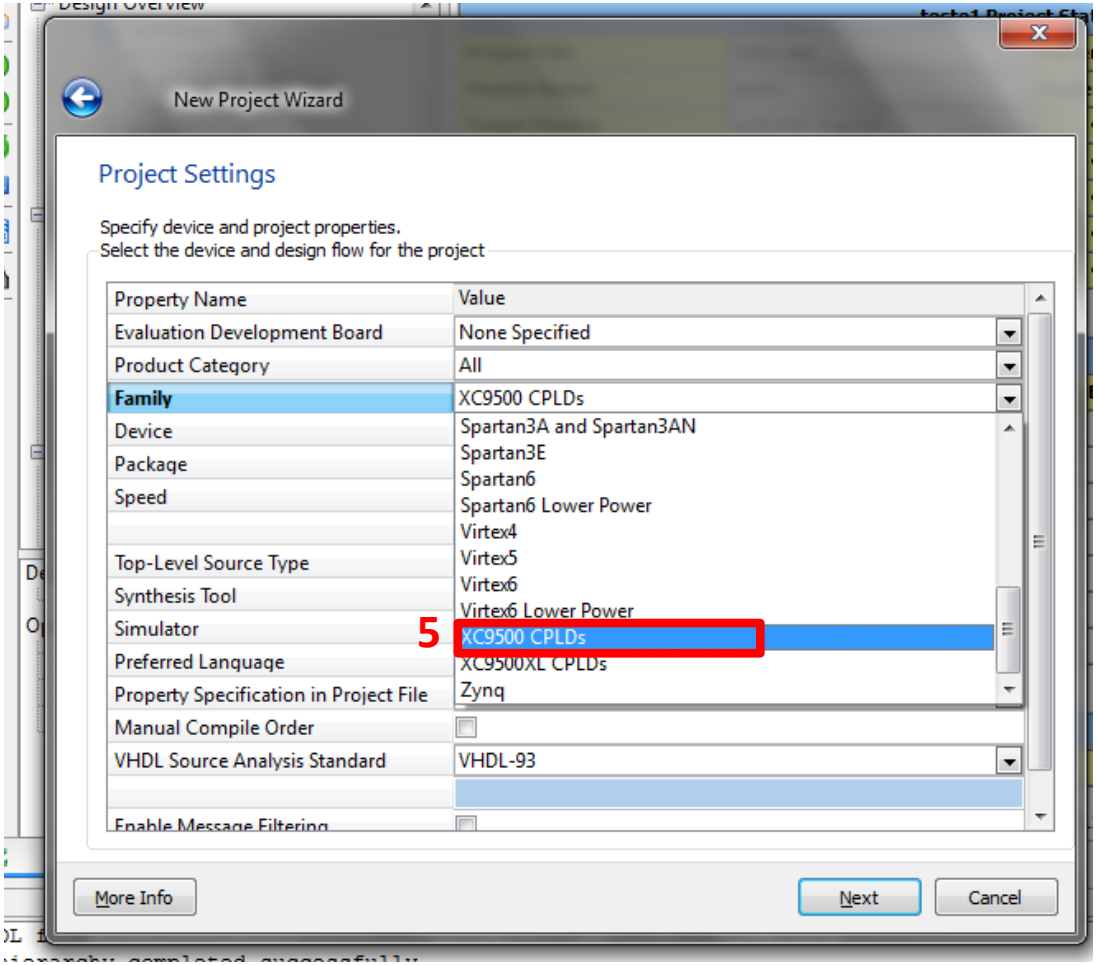


3-Dar o nome ao projecto

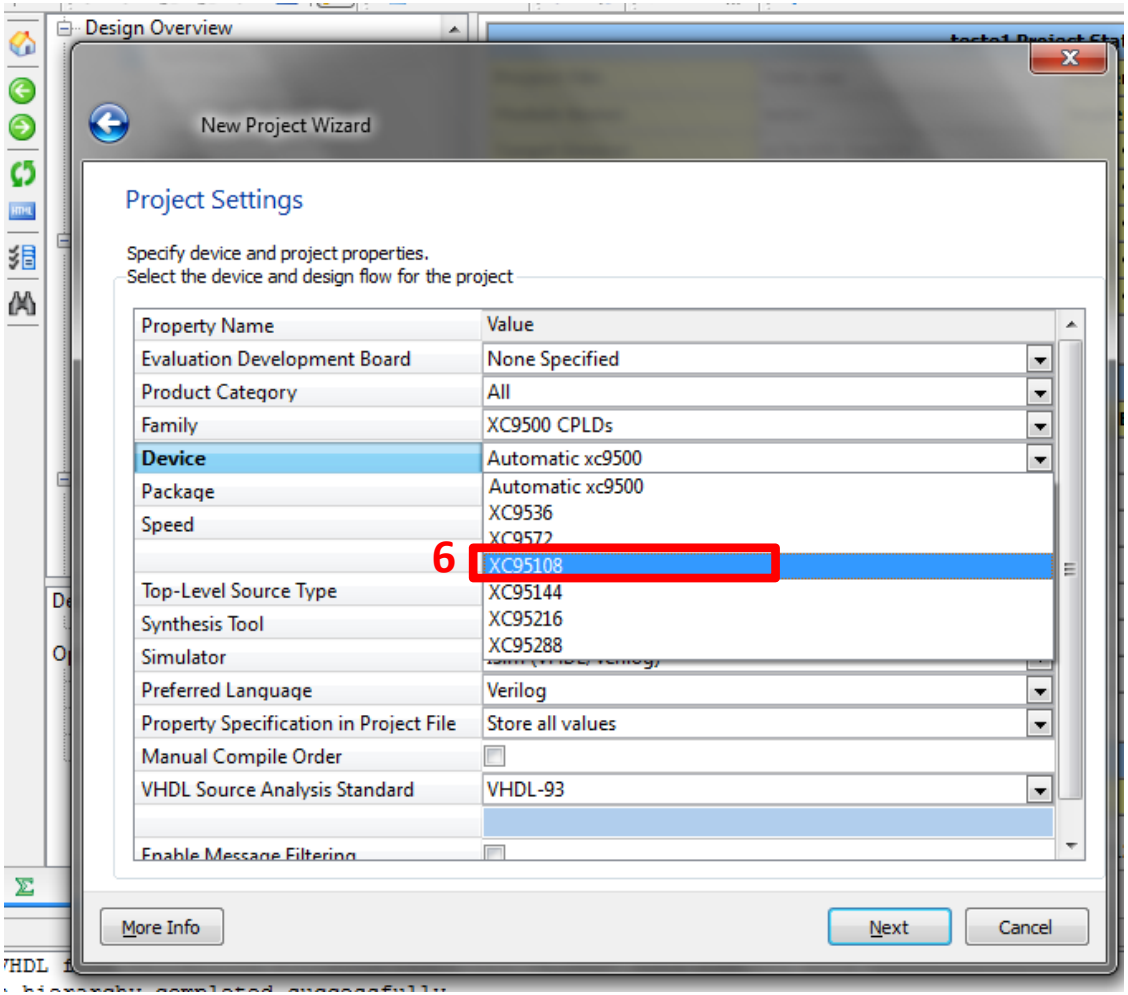
4- Next



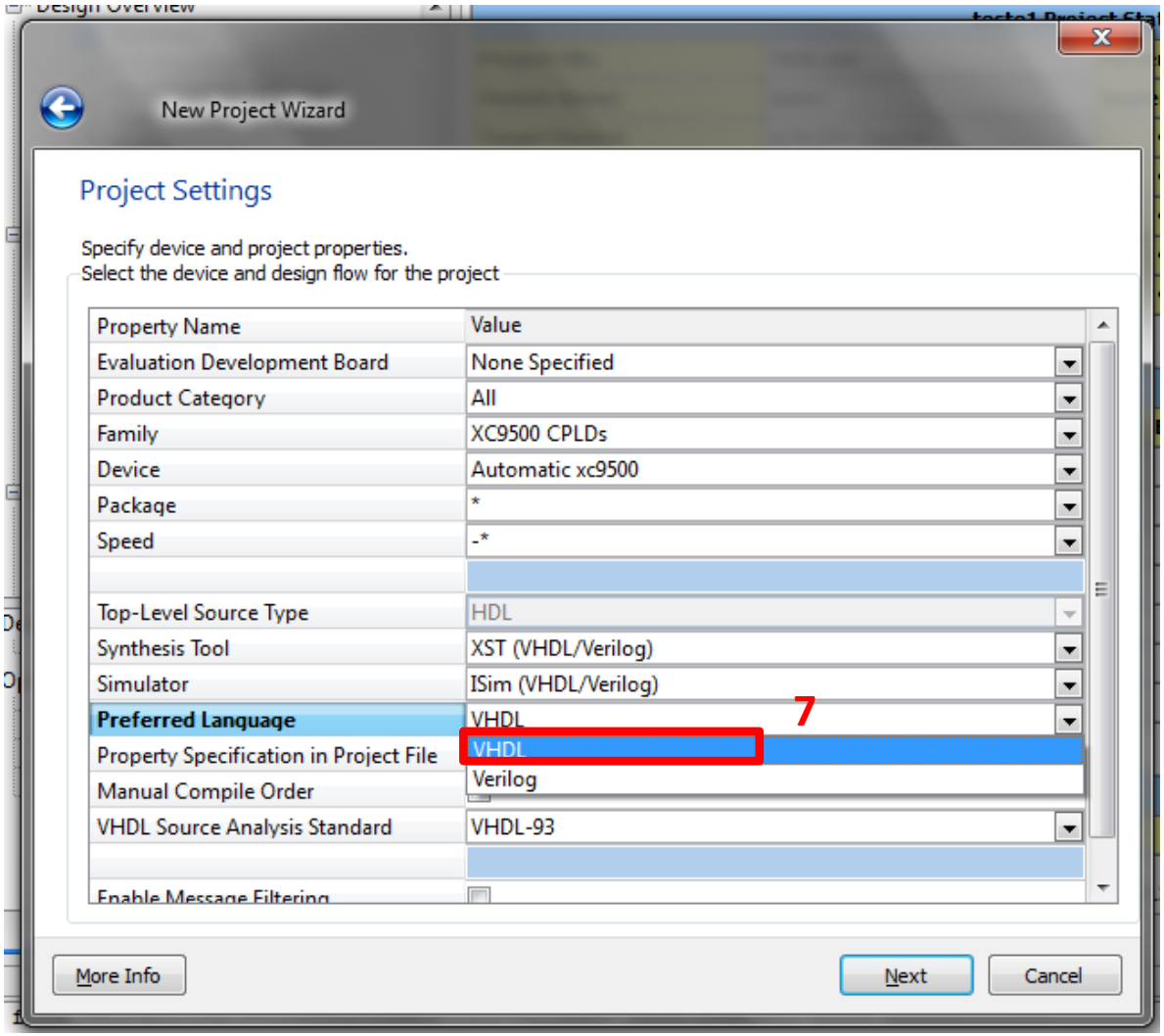
5- No campo Family escolher XC9500 CPLDs



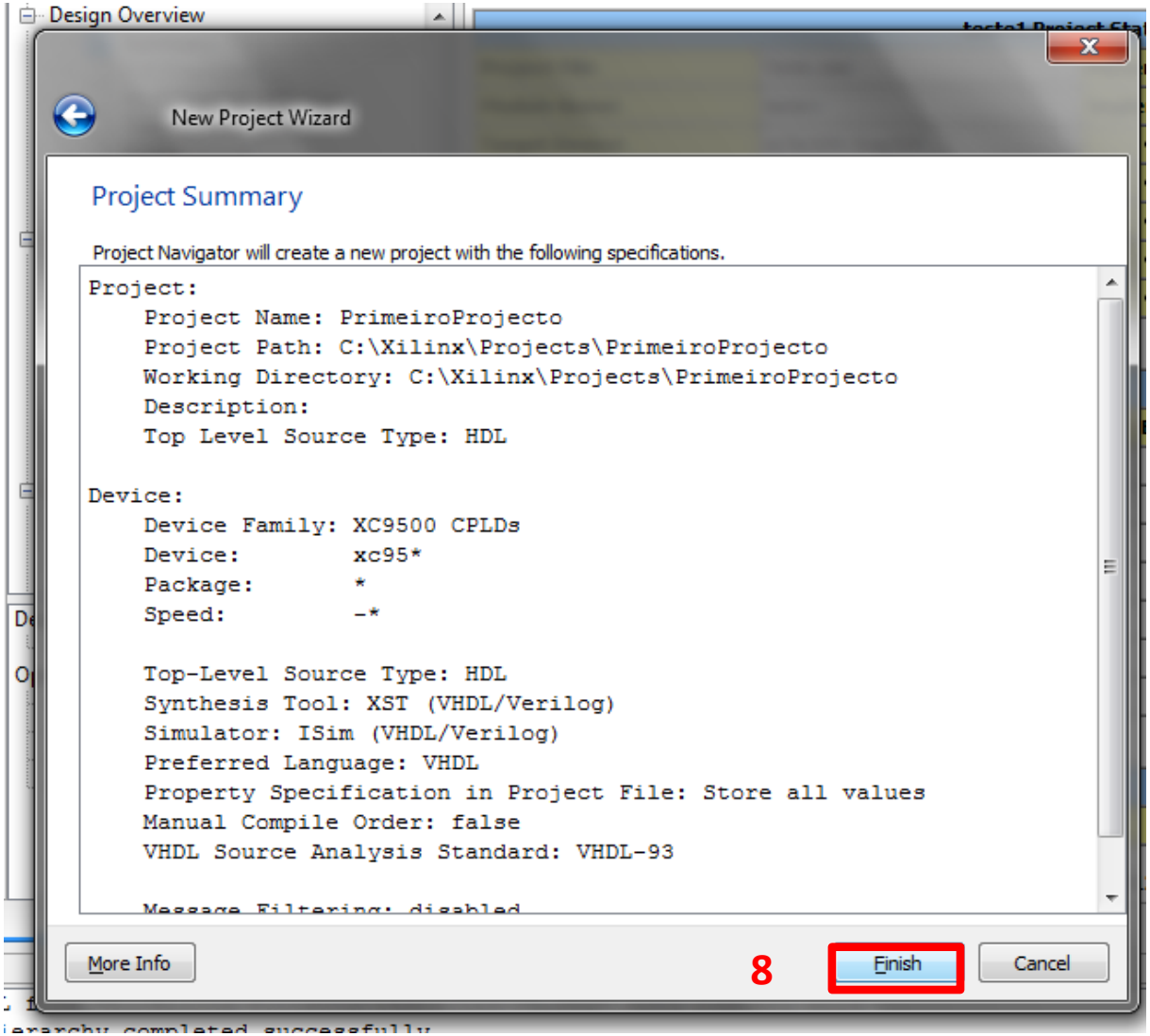
6- No campo Device escolher o XC95108



7- No campo Prefered Language escolher VHDL



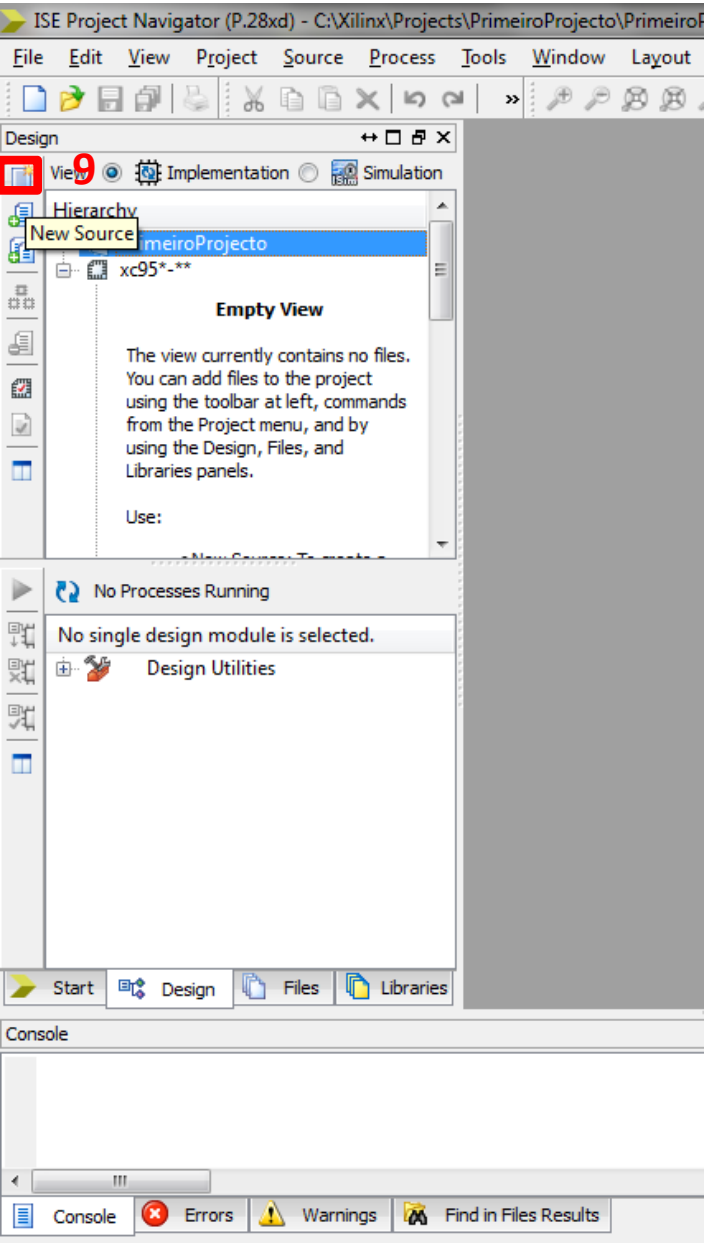
8- Finish

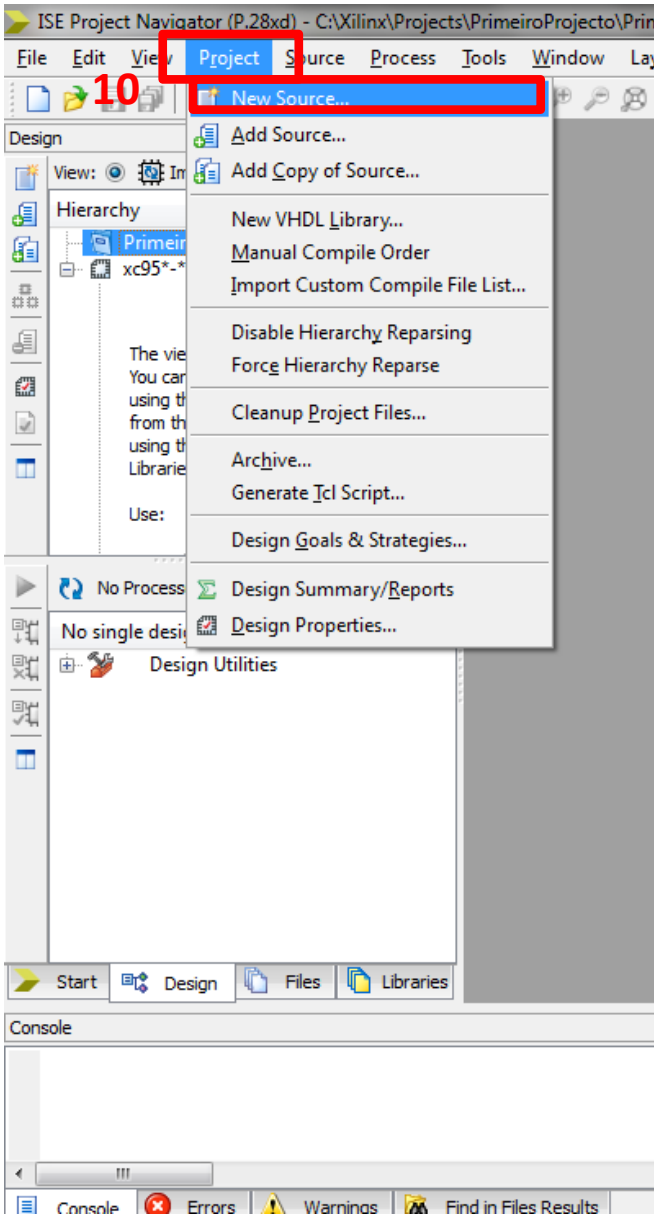

Design Overview
New Project Wizard
Project Summary
Project Navigator will create a new project with the following specifications.
Project:
Project Name: PrimeiroProjecto
Project Path: C:\Xilinx\Projects\PrimeiroProjecto
Working Directory: C:\Xilinx\Projects\PrimeiroProjecto
Description:
Top Level Source Type: HDL
Device:
Device Family: XC9500 CPLDs
Device: xc95*
Package: *
Speed: -*
Top-Level Source Type: HDL
Synthesis Tool: XST (VHDL/Verilog)
Simulator: ISim (VHDL/Verilog)
Preferred Language: VHDL
Property Specification in Project File: Store all values
Manual Compile Order: false
VHDL Source Analysis Standard: VHDL-93
More Info
8
Finish
Cancel

9- Clicar no botao New Source

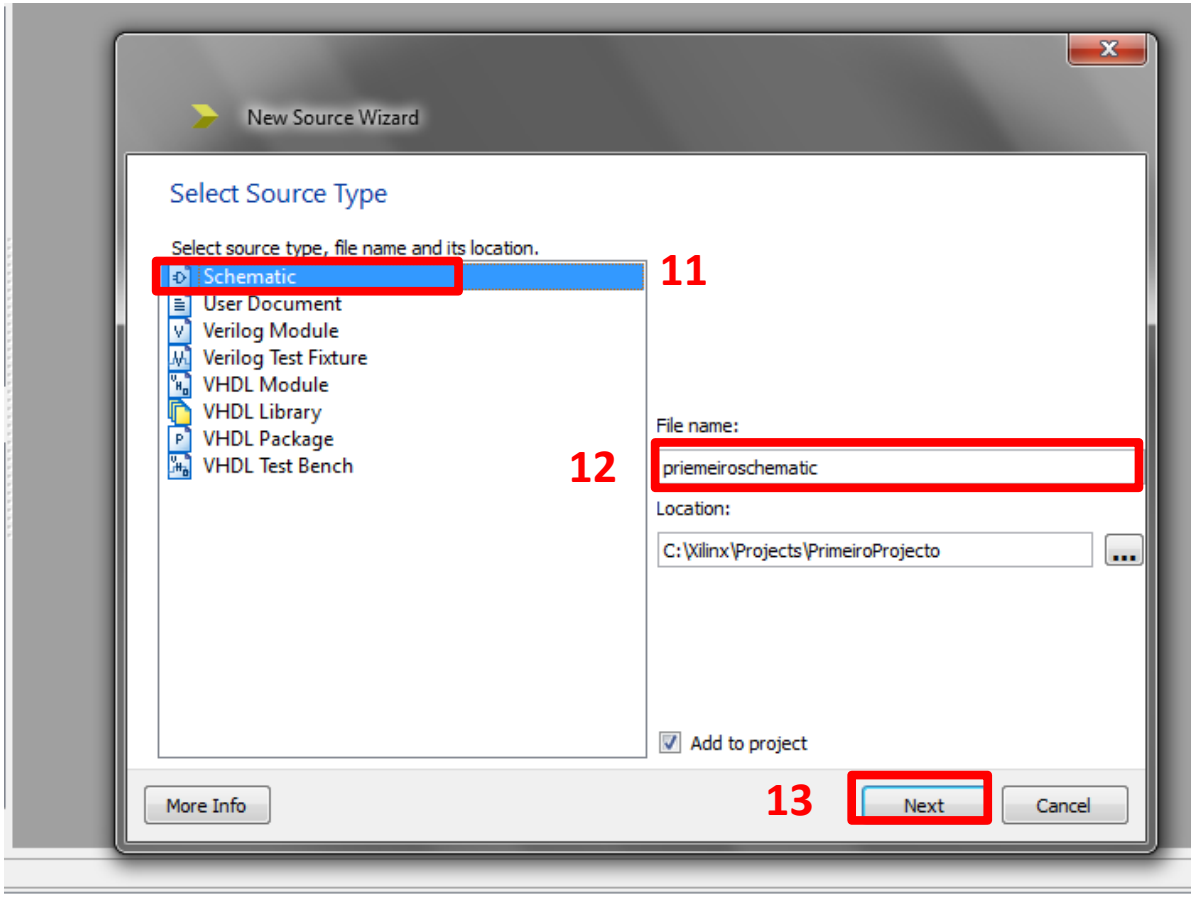
OU

10- Em Project, clicar em New Source



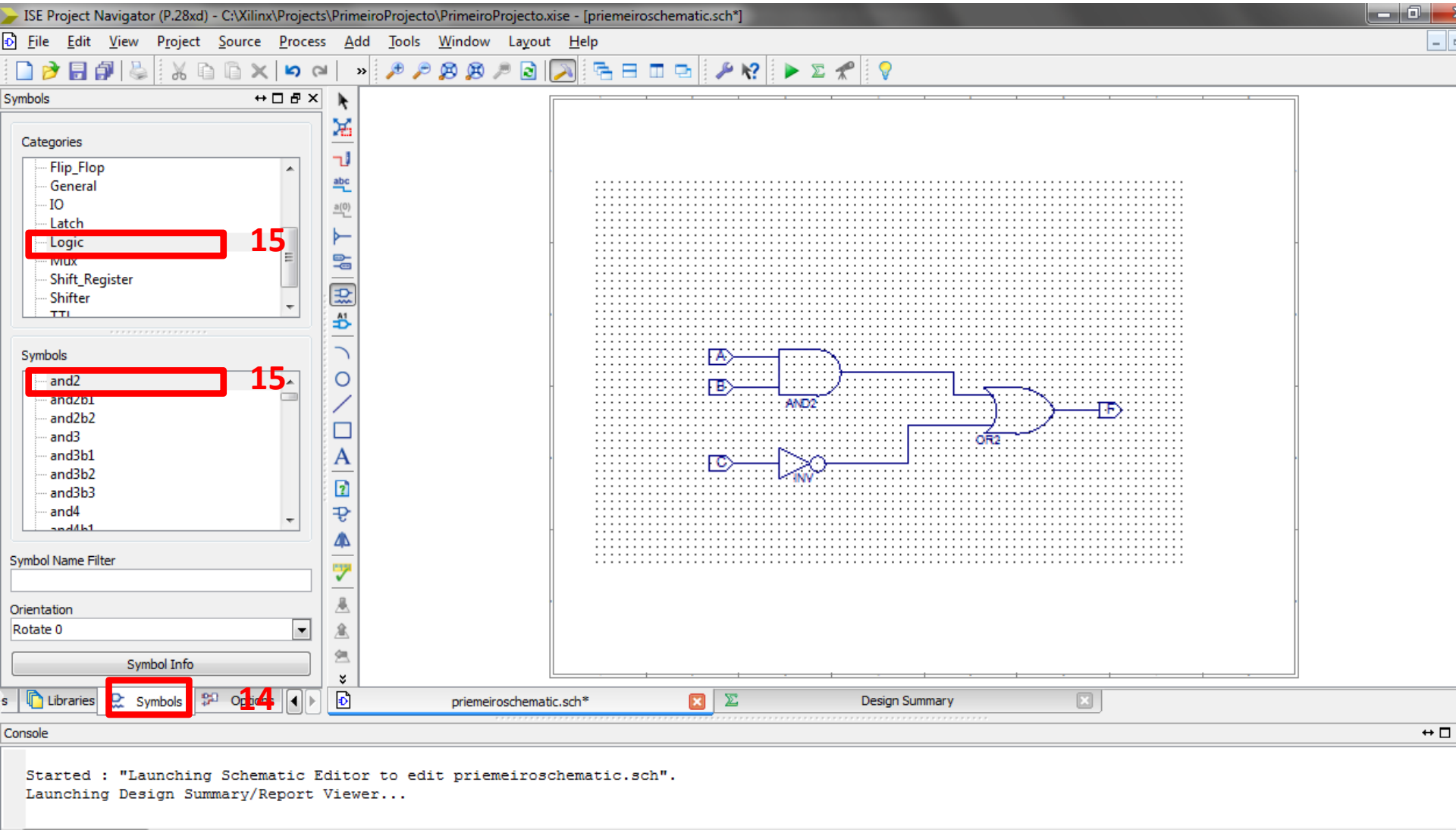


11- Escolher Schematic para criar um esquemático
12- Dar um nome ao ficheiro
13- Next

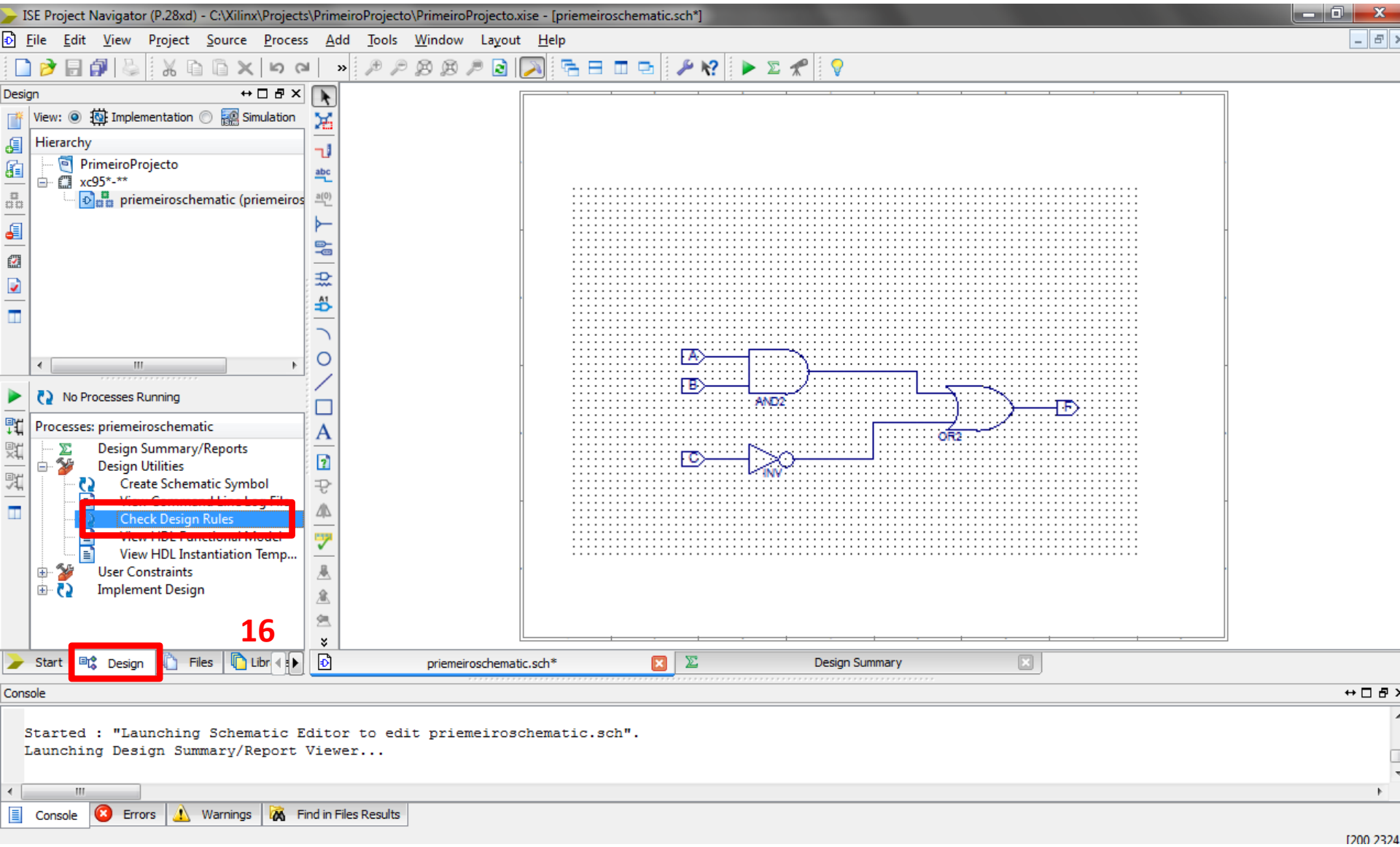


14- Clicar na tab de Symbols, e escolher que simbolos colocar.

15- Exemplo: escolher Logic e depois uma and2 (And 2 entradas)



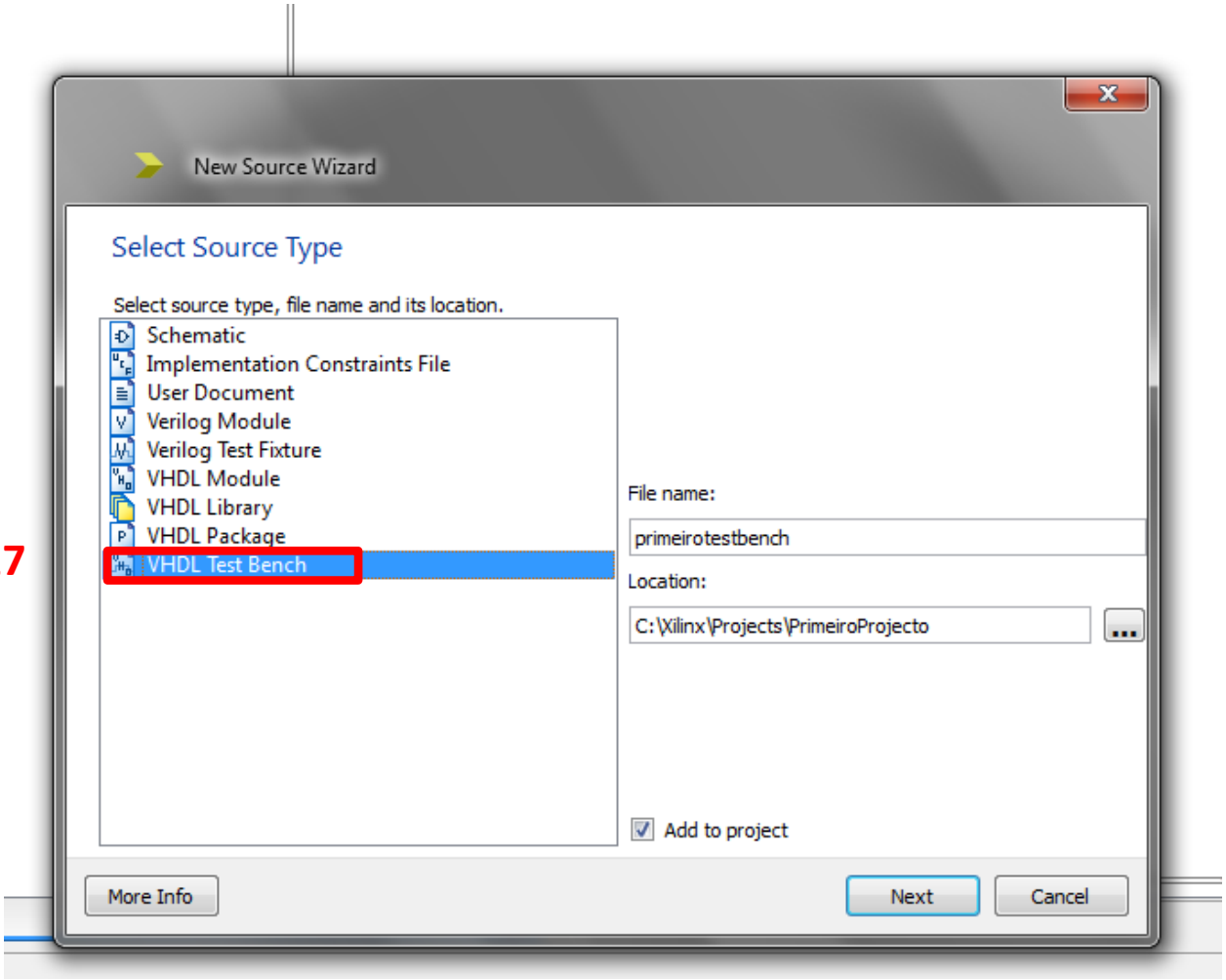
16- Para verificar se todas as ligações estão correctas, em Design, Design Utilities, Check Design Rules.



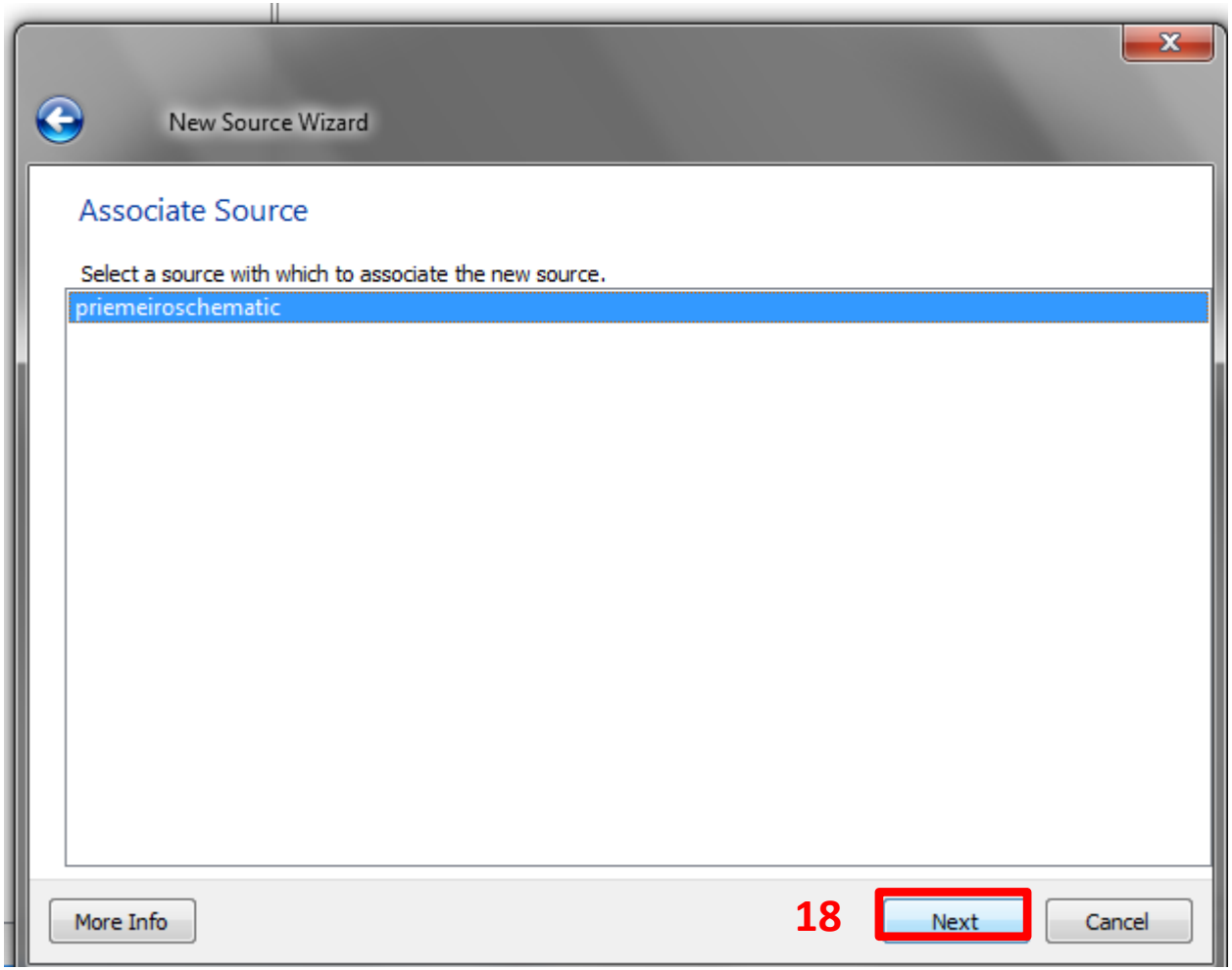
Como criar um ficheiro de simulação

17- Clicar em New Source como feito no passo 9 ou 10, e escolher VHDL Test Bench

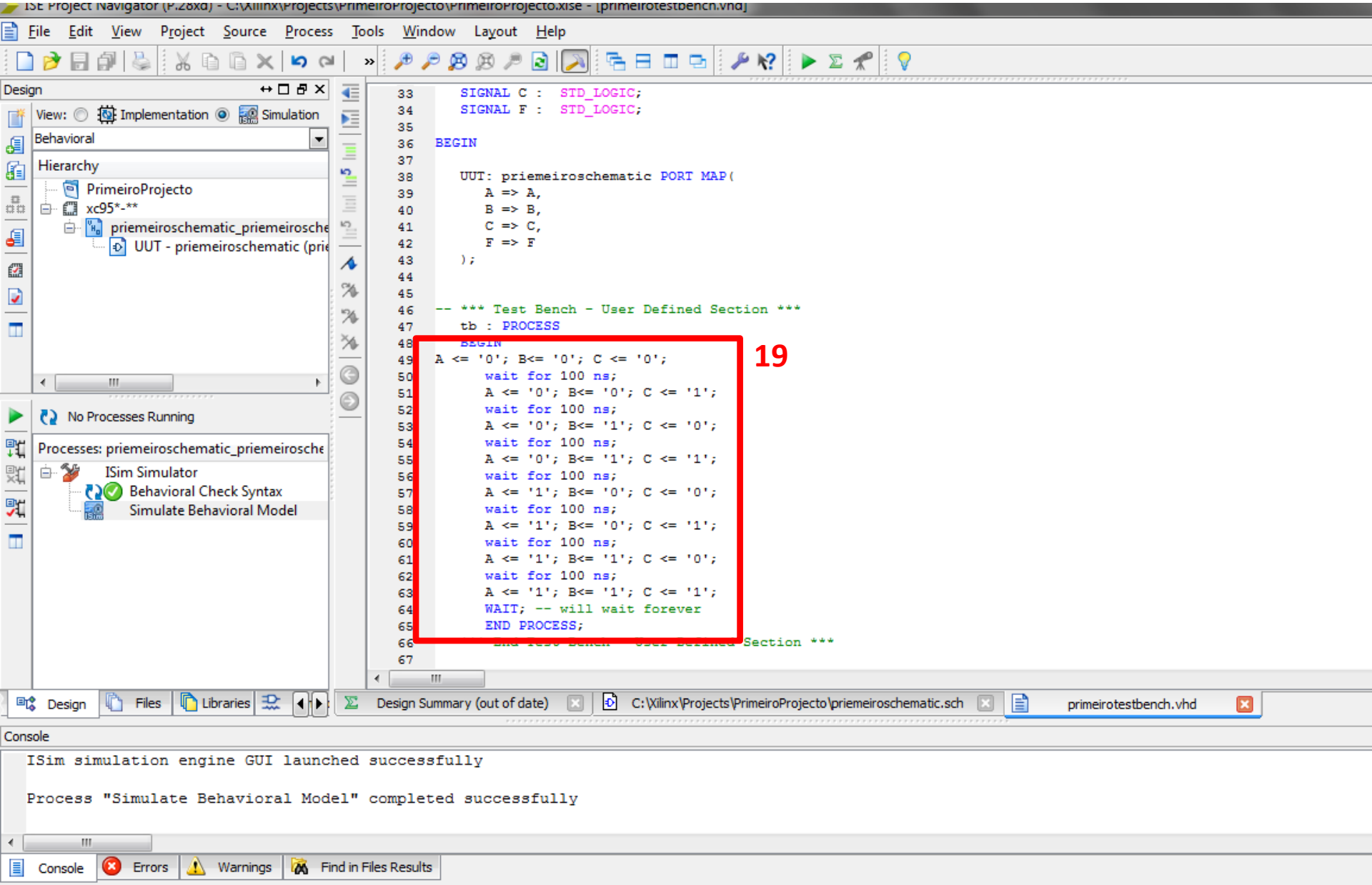
17



18- Escolher da lista de esquemáticos o esquemático que queremos simular. (um projecto pode conter vários esquemáticos) e clicar em next. Isso vai criar um ficheiro de simulação em VHDL que vamos ter de modificar.



19- No ficheiro criado é necessário introduzir a evolução das entradas. Um exemplo para 3 bit está apresentado no quadro 19.



20- Para obter o gráfico, em Simulation, clicar em Behavioral Check Syntax e depois em Simulate Behavioral Model e uma nova janela aparecerá com o gráfico temporal.